Physics Notes

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Class:10+2

Unit: IX

Topic: Electronic Devices

SYLLABUS: UNIT-IX

Semiconductors; semiconductors diode – I-V characteristics in forward and reverse bias, diode as a rectifier; I-V characteristics of LED, photodiode, solar cell and Zener diode; Zener diode as a voltage regulator. Junction transistor, transistor action, characteristics of transistor; transistor as an amplifier (common emitter configuration) and oscillator. Logic gates (OR, AND, NOT, NAND and NOR). Transistor as a switch.

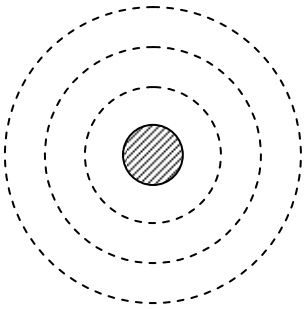
	Unit – 9C(Logic Gates)	
1.	Use NAND Gate to make a) NOT GATE b) AND GATE c) OR GATE	
2.	Use NOR Gate to make a) NOT GATE b) AND GATE c) OR GATE	
3.	De-Morgan's theorem?	

Unit – 9A(Solids and Semi Conductor Devices)

Q.1. Discuss

a) Energy diagram for isolated atom.

b) Energy bands for material (Group of Atoms).

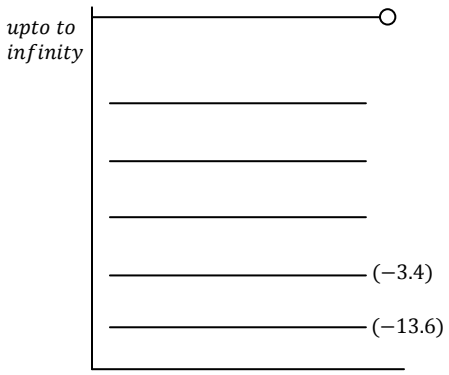


Ans Electrons can have discrete values

$E_n = \frac{-13.6\ eV}{n^2}$ in isolated atoms

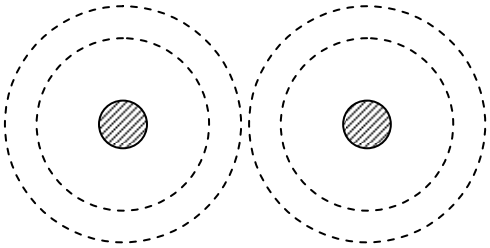
$2\pi R = n\lambda$

When the atoms are placed close in material, there is no appreciable modification in the energy levels of electrons in the inner shells but there is a considerable modification in the case of energy levels of the electrons in the outer shells.



(i) If the interatomic spacing of the atom is very large(r=d>>a), there is no interatomic interaction. Each atom in the crystal behaves as free atom

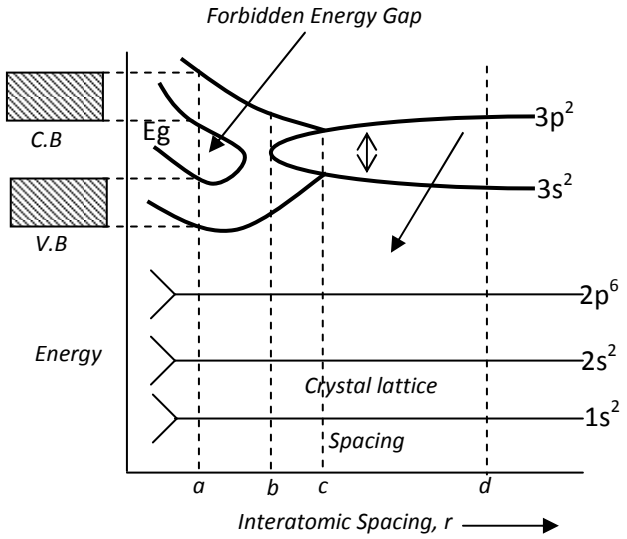
(ii) When the interatomic spacing r is less than d but greater than c (i.e. c < r < d), there is no visible splitting of energy levels.



(iii) When the interatomic spacing r is equal to c, the interaction between outermost shell electrons ($3s^2$ and $3p^2$) of neighbouring silicon atoms becomes appreciable

(iv) When the ineratomic spacing r lies in between b and c (i.e. b <r <c), the energy of electrons corresponding to 3s and 3p levels of each atom gets slightly changed.

(v) When the interatomic spacing r becomes equal to b but greater than a (i.e. r = b > a), the energy gap between 3s and 3p levels completely disappears and the 8N energy levels are continuously distributed. In such a situation, it is not possible to distinguish between the electrons belonging to 3 s and 3p sub shells. We can only say that 4N levels are filled and 4N levels are empty.



Q2. Explain behavior of

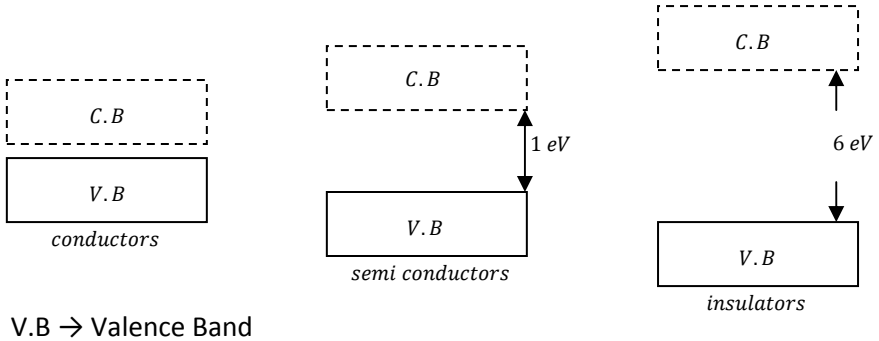
a) Conductors

b) Semi conductors

c) Insulators

On the basis of Energy band/Forbidden Gap.

Ans.



V.B → Valence Band

C.B → Conduction Band

<u>Conductors</u>:

V.B and C.B-Gap is either very low or zero. Electrons can move to C.B without any extra energy at room temperature, So they can move freely inside the material and offer no opposition to flow of current. So, resistance of conductors is low.

<u>Semi Conductors</u>:

V.B and C.B-Gap is low. Electrons can move to C.B with an energy of 1 eV at room temperature. So they can move freely inside the material and offer moderate opposition to flow of current. So resistance of semi conductors is high as compared to conductors.

<u>Insulators</u>:

V.B and C.B-Gap is very high. Electrons require a high energy of 6 eV. At room temperature this much high energy is not available. So C.B remains free of electrons under normal conditions.

<u>AIR</u>:

Conductivity of air depends upon the conditions. At room temperature, air is an insulator. But when high voltage is applied, air behaves as a conductor due to ionization of air.

Q3. a) What is a "hole" in semi conductor?
b) Formation of hole.
c) Direction of movement of hole?

Ans. *Si – Si* covalent bond is formed as shown in Fig I. Under suitable conditions, electron moves out from *Si Si* bond and creates a vacancy.

"*This vacancy*" is termed as a *hole*".

This vacancy has the tendency to attract other electrons and achieve stable state.

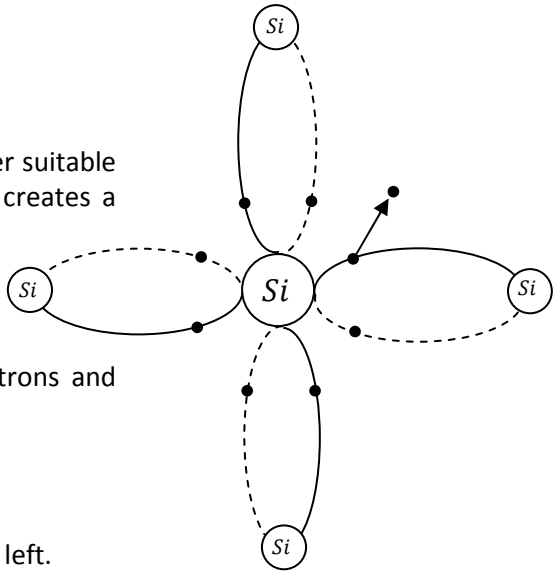


Fig. I

Direction of movement of hole:

Electrons move to right and vacancy i.e. holes move to left.

I = $|I_e|$ + $|I_h|$ (see Fig. IV)

= 2 + 3

= 5

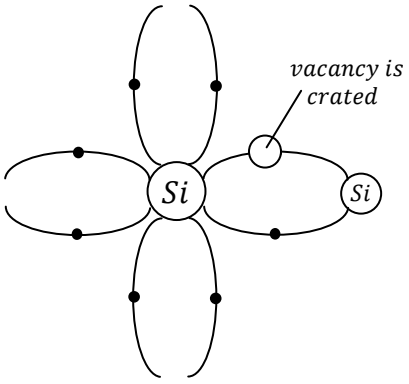


Fig. II

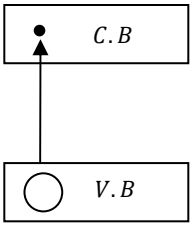


Fig. III

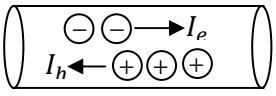


Fig. IV

Q4. Compare Intrinsic semi conductors and Extrinsic semi conductors?

Ans.

Intrinsic	Extrinsic
1. It is a **pure** semi conducting material.	1. It is prepared by doping.
2. Example are pure silicon and germanium.	2. Example are silicon and germanium crystals with impurity atoms of arsenic, antimony and phosphorus.
3. The number of free electrons in conduction band and number of holes in valence band is exactly equal.	3. Number of free electrons and holes is never equal.
4. Its electrical conductivity is low.	4. Its electrical conductivity is high.
5. Its electrical conductivity is a function of temperature alone.	5. Electrical conductivity depends upon the temperature as well as on the quantity of impurity.

Periodic table part of semi conductors

B	C	N
	Si	
	Ge	

Q5. What is Doping? Essential conditions for doping?

Ans. Doping is a process of deliberate addition of a desirable impurity atoms to a pure semiconductor to modify its properties in a controlled manner. The impurity atoms added are called do-pants.

In a doping process, it is required that:

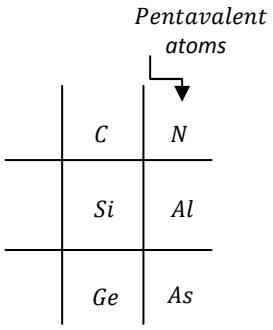
1. The do-pant atom should take the position of semiconductor atom in the lattice.
2. The presence of the do-pant atom should not distort the crystal lattice.
3. The size of the do-pant atom should be almost the same as that of the crystal atom.
4. The concentration of do-pant atom should not be large (not more than 1% of the crystal atom).

Q6. Discuss

a) N-type semiconductor

b) P-type semiconductor

Compare the two.

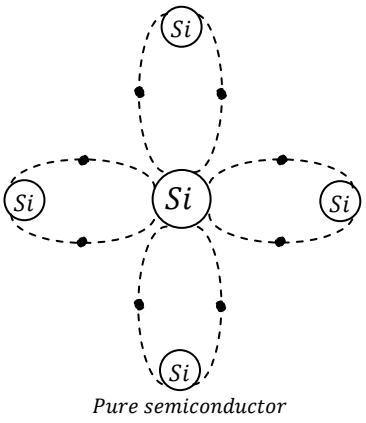


Ans. **<u>N-type semiconductor</u>**:

It doped with a controlled amount of pentavalent atoms. Impurity atoms which donate free electrons for conduction are called *Donor Atoms*.

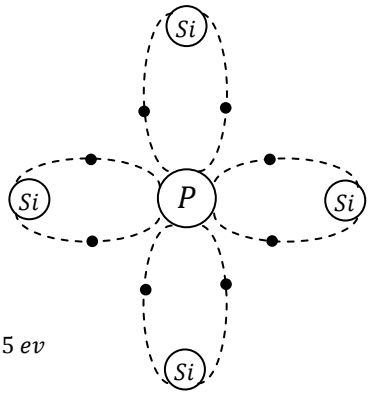
The resulting semiconductor is called N-type semiconductor.

The extra electrons of the donor atom orbits around the donar nucleus, in a hydrogen like manner.

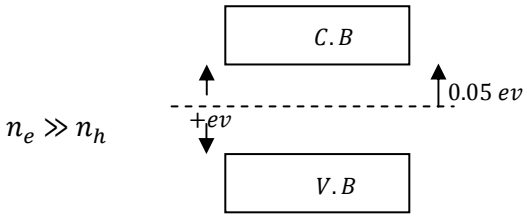


Pure semiconductor

It has been found that 0.05 eV energy in *Si* is required to remove this election from the impurity atom and makes it a free electron. The total number of holes in N-type semiconductor is relatively low, hence in N-type semiconductor, Electrons are majority carriers and holes are minority carriers.



These electrons occupy discrete energy levels (called donor energy levels) between the valence and conduction band and the lowest donor electron energy level lies at 0.05 eV below the bottom of the conduction band.



$n_e \gg n_h$

P-type semiconductor:

The trivalent atoms are called acceptor atoms and the conduction of electricity occurs due to motion of holes i.e. positive charges or P-type carriers. That is why the resulting semiconductor is called acceptor type or P-type semiconductor.

Q7. Conductivity for semi conductors?

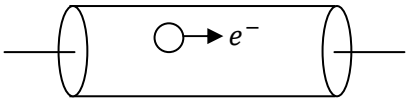
Ans.

a) Conductors

$\sigma = \frac{ne^2\tau}{m} = ne\left(\frac{e\tau}{m}\right) = n_e\mu$ $\quad \begin{bmatrix} \sigma \rightarrow conductivity \\ \mu \rightarrow mobility \\ \mu \rightarrow \frac{e\tau}{m} \end{bmatrix}$

b) Semi Conductors

Conductivity = conductivity due to electrons + Conductivity due to holes i.e.



$\sigma = \sigma_e + \sigma_h$

$= \left(\frac{ne^2\tau}{m}\right)_{electrons} + \left(\frac{ne^2\tau}{m}\right)_{holes}$

$= (n_e\mu)_e + (n_e\mu)_h$

$= n_e\,\mu_e\,e + n_h\,\mu_h\,e$ $\quad \begin{bmatrix} \mu_e \rightarrow \text{mobility of electrons} \\ \mu_h \rightarrow \text{mobility of holes} \end{bmatrix}$

<u>Case I</u>: N-type semiconductors (Electrons are in majority, holes in minority)

$\sigma \simeq n_e\,\mu_e\,e + 0$

$\simeq N_d\,\mu_e\,e + 0$ (N_d, No. of donor atoms = No. of electrons as each donor one electron contributes)

$\boxed{\sigma_n \simeq N_d\,\mu_e\,e}$

<u>Case II</u>: P-type semiconductors (Holes are in majority, electrons in minority)

$\sigma \simeq 0 + n_h\,\mu_h\,e$

$\simeq 0 + N_A\,\mu_h\,e$ (N_A, No. of acceptor atoms = No. of holes as each acceptor atom creates one hole)

$\boxed{\sigma_n \simeq N_A\,\mu_h\,e}$

This is obtained when Si or Ge is doped with a trivalent impurity like AI, B, In, etc. The dopant has one valence electron less than Si or Ge and, therefore, this atom can form covalent bonds with nighbouring three Si atoms but does not have any electron to offer to the fourth Si atom. So the bond between the fourth nighbour and the trivalent atom has a vacancy or hole as shown in Fig. Since the nighbouring Si atom in the lattice wants an electron in place of a hole. An electron in the outer orbit of an atom in the neighbourhood may jump to fill this vacancy, leaving a vacancy or hole at its own site. Thus the hole is available for conduction. Note that the trivalent foreign atom becomes effectively negatively charged when it shares fourth electron with neighbouring Si atom. Therefore, the dopant atom of p-type material can be treated as core of one negative charge along with its associated hole as shown in Fig. It is oabvious that one acceptor atom gives one hole. These holes are in addition to the intrinsically generated holes while the source of conduction electrons is only intrinsic generation. Thus, for such a material, the holes are the majority carriers and electrons are minority carriers. Therefore, extrinsic semiconductors doped with trivalent impurity are called p-type semiconductors. For p-type semiconductors, the recombination process will reduce the number (n_i) of intrinsically generated electrons to n_e. We have, for p-type semiconductors.

$n_h \gg n_e$

Note that the crystal maintains an overall charge neutrality as the charge of additional charge carriers is just equal and opposite to that of the ionized cores in the lattice.

In extrinsic semiconductors, because of the abundance of majority current carriers, the minority carriers produced thermally have more chance of meeting majority carriers and thus getting destroyed. Hence, the dopant, by adding a large number of current carriers of one type, which become the majority carriers, indirectly helps to reduce the intrinsic concentration of minority carriers.

The semiconductor's energy band structure is affected by doping. In the case of extrinsic semiconductors, additional energy states due to donor impurities (E_D) and acceptor impurities (E_A) also exist. In the energy band diagram of n-type Si semiconductor, the donor energy level E_D is slightly below the bottom E_C of the conduction banc and electrons from this level move into the conduction band with very small supply of energy. At room temperature, most of the donor atoms get ionized but very few $(\sim 10^{-12})$ atoms of Si get ionized. So the conduction band will have most electrons coming from the donor impurities, as shown in Fig. Similarly, for p-type semiconductor, the acceptor energy level E_A is slightly above the tope E_V of the valence band as shown in Fig. With very small supply of energy an electron from the valence band can jump to the level E_A and ionise the acceptor negatively. (alternately, we can also say that with very small supply of energy the hole from level E_A sinks down into the valence band. Electrons rise up and holes fall down when they gain external energy.) At room temperature, most of the acceptor atoms get ionised leaving holes in the valence band. Thus at room temperature the density of holes in the valence band is predominantly due to impurity in the extrinsic semiconductor. The electron and hole concentration in a semiconductor in thermal equilibrium is given by

$n_e n_h = n_i^2$

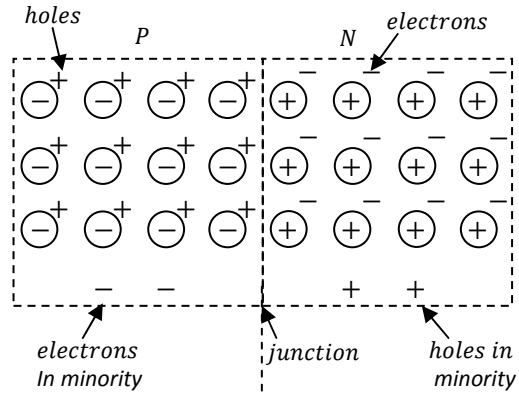
Though the above description is grossly approximate and hypothetical. It helps in understanding the difference between metals, insulators and semiconductors (extrinsic and intrinsic) in a simple manner. The difference in the resistivity of C, Si and Ge depends upon the energy gap between their conduction and valence bands. For C (diamond), Si and Ge, the energy gaps are 5.4 eV and 0.7 eV, respectively, Sn also is a group IV element but it is metal because the energy gap in its case is 0 eV.

Unit – 9B

Q1. a) Formation of P-N junction?
b) "Potential Barrier" and "Depletion Layer"?
c) "Drift Current" and "Diffusion Current"?

Ans.

a) P-type material (holes in majority) is placed in contact with N-type material (e^- in majority). Electrons move from N-type to P-type to combine with holes. P-side of junction gets negative charge and N-side of junction gets positive charge. Such a junction is called *P-N junction*.

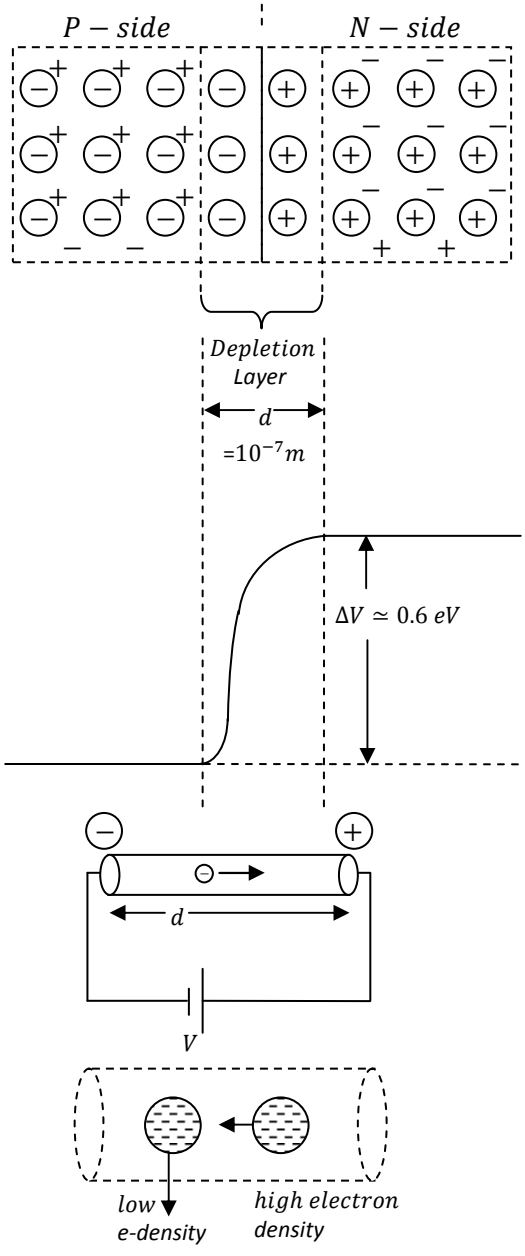


b) The central part of width d is depleted of free charge carriers. This part is called "*Depletion Layer*".

$$C_{depletion\ layer} = \frac{\in_0 A}{d}$$

Electrons in N-type experience repulsive force due to negative face of P-side Kinetic Energy required by electrons to overcome this potential barriers is of the order 0.6 eV.

Similarly, holes in P-side need 0.6 eV to cross to the other side. This energy required (0.6 eV) is termed as *Potential Barrier*.



c) **Drift, Diffusion Current**:

Drift Current

e^- moves under electric filed, current is called *Drift Current*.

$$E = \frac{v}{d}$$

Diffusion Current

e^- move from high electron density to low e^- density, current flowing is called *Diffusion Current* i.e. Flow of electrons due to density gradient is called diffusion current.
In a P-N junction under equilibrium, drift current is equal to diffusion current. So, net current is *ZERO*.

Q2. What is Biasing? Draw circuit diagram and explain

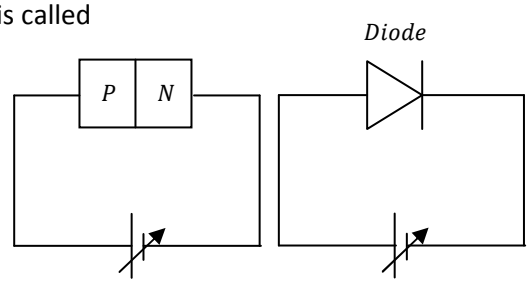
a) Forward Biasing of a diode

b) Reverse Biasing of a diode

Also draw its characteristics?

Ans. The process of placing voltage across a diode, transistor is called *Biasing*.

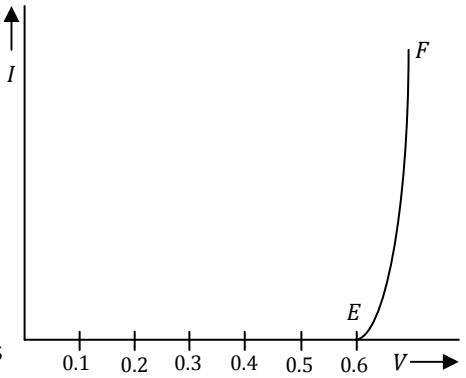
a) **Forward Biasing of a Diode**:



In forward Biasing, positive terminal of the battery is connected to P-side and negative terminal is connected to N-side of diode.

Characteristics:

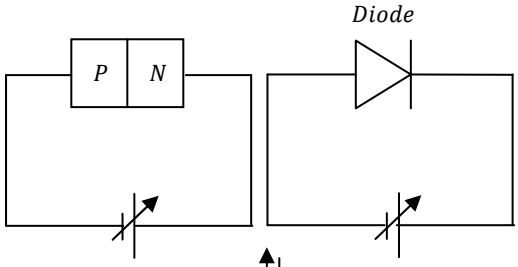
Apply a voltage 0.1 V. Energy available with a hole 0.1 eV is less than Potential Barrier of 0.6 eV. So, hole cannot cross to an N-side. So, current passing is almost zero. When the applied voltage is 0.6 V or more, current flows across P-N junction.



I-V characteristics is as shown in the figure (non-ohmic characteristic in which V α I is not valid).

b) **Reverse Biasing of a Diode**:

In reverse Biasing, negative terminal of the Battery is connected P-side and positive terminal is connected to N-side.



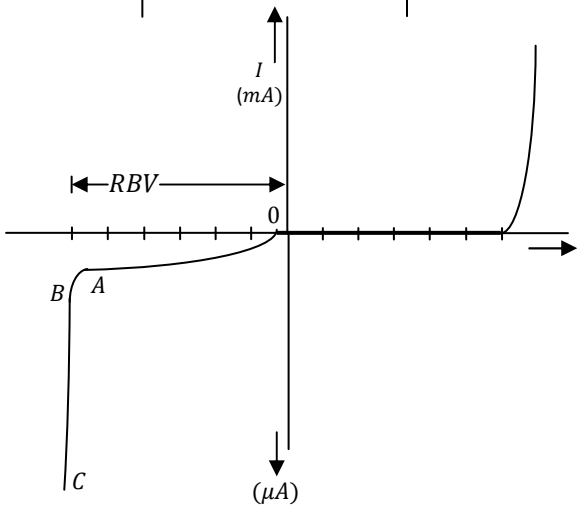
Negative terminal of the Battery will attract holes in P-side and positive terminal of the battery will attract electrons on N-side. So, holes in P-side and electrons in N-side move away from junction.

So, Depletion Layer width increase.

Capacitance of a diode decrease

As $C = \frac{E_0 A}{d}$

Electrons in P-side (minority carriers) move towards the junction, holes in N-side (minority carriers) move towards the junction. So, current flows due to minority carriers in reverse Biasing.



If reverse voltage goes on increasing, a stage is reached where electrons get detached from parent atom and diode becomes a conductor.

Heavy current causes damage to diode and gets burned. Part BC of characteristic shows heavy current. Normal diodes are never operated in this zone BC.

RBV → Reverse Breakdown Voltage

Q3. Construction, Working of "Half-Wave Rectifier".

Ans. Half Wave Rectifier is a device which is used to rectify *+ve* half cycles of input alternating current. Output corresponding to *–ve* half cycles is zero. (*Fig. I*)

Fig. I

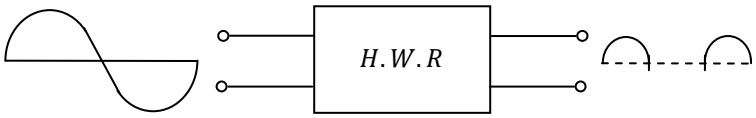
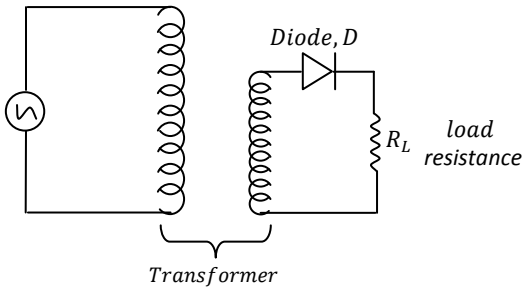


Fig. II



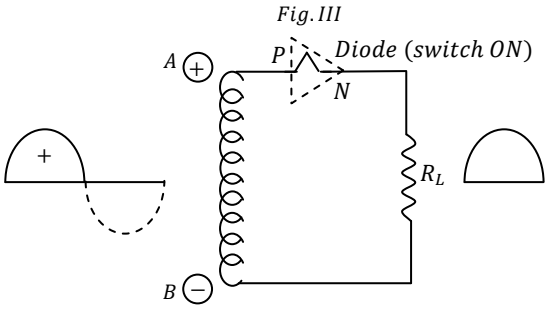
Construction:

Alternating current/voltage is given to a transformer. Transformer changes the voltage level. Output of Transformer is connected to load resistance through a diode, *D* as shown in *Fig. II*.

Working:

During, *+ve* half cycle, upper end *A* of transformer secondary is *+ve* w.r.t lower end *B*. As *A (+ve)* is connected to P-side of diode, *D*, diode gets forward biased. In forward Biased Diode acts as "ON" Switch. Voltage across *AB* is available across R_L with same variation. So, *+ve* half cycle gets transferred to R_L as shown in Fig. III.

Fig. III

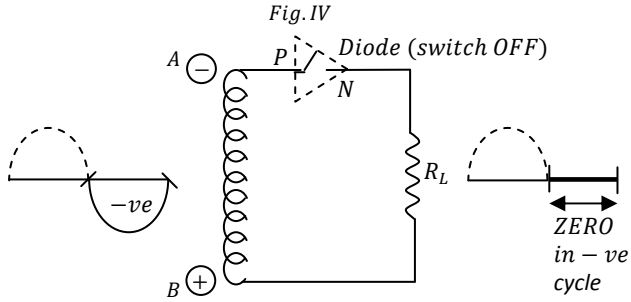


During *–ve* half cycle, upper end *A* of transformer secondary is *–ve* w.r.t. lower end *B*. As *A (-ve)* is connected to P-side of Diode *D,* Diode is Reverse Biased.

In Reverse Biased Diode acts as OFF Switch.

Current flowing is zero, so voltage across load resistance (R_L) is zero, as shown in Fig. IV.

Fig. IV



Q4. Construction, Working of "Full-Wave Rectifier".

Ans. Full Wave Rectifier is a device which is used to rectify *+ve* half cycle and *–ve* half cycle of input alternating current.

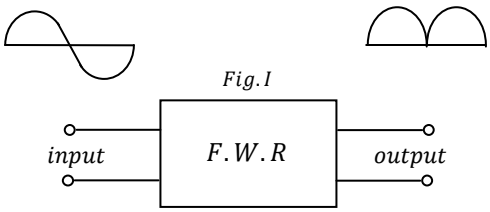


Fig. I

Construction:

Alternating current voltage is given to transformer. Transformer changes the voltage level. Two diodes D_1 and D_2 are connected to a load resistance. A wire is taken from centre of secondary transformer. So, it is called centre tapped transformer.

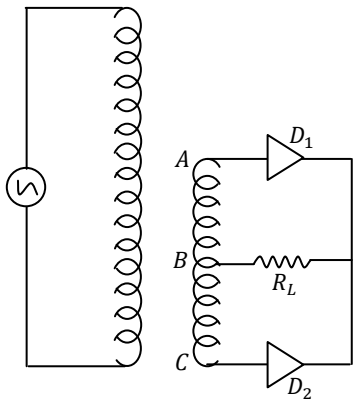


Fig. II

Working:

During *+ve* half cycle, upper end *A* of transformer secondary is *+ve* is connected to P-side of Diode D_1, diode D_1 get forward biased and D_2 gets reverse biased, so D_2 is OFF. Current flows in R_L from right to left (Fig.III)

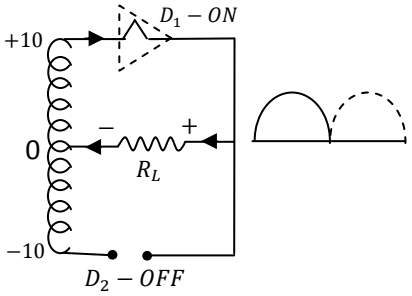


Fig. III

During *–ve* half cycle, lower end *+ve* and upper end *–ve*. So D_2 acts as Forward Biased and Switch is ON and current in R_L flows from right to left, Whereas Diode D_1 acts as Reverse Biased and Switch is OFF, so wave shape of voltage across R_L is as shown in *Fig. IV*.

So, both halves are rectified such that current flows through R_L in same direction in both +ve and –ve half cycles.

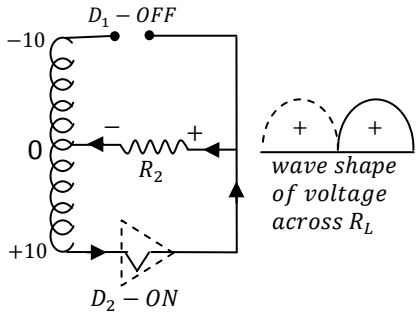


Fig. IV

23,1

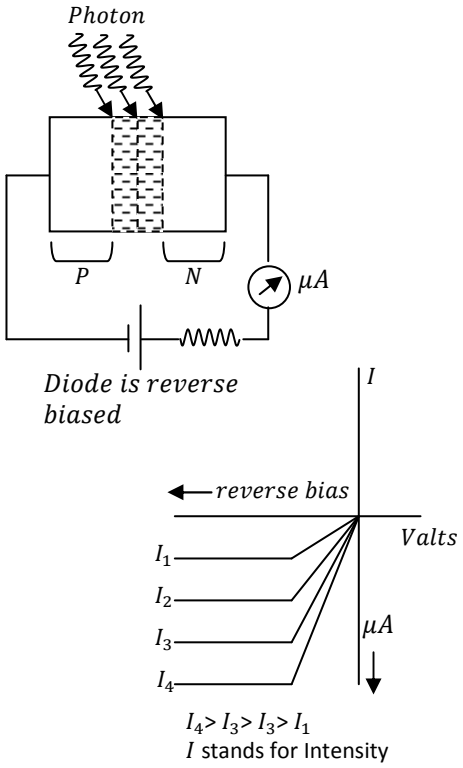
Q5. a) What are different types of diodes?

b) Use "Zener Diode" as a voltage stabilizer".

Ans.a) Different types of diodes → Photodiodes, LED, Solar Cell
Optoelectronic Devices:

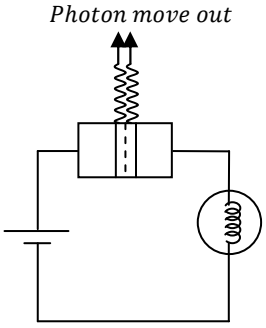
1. **Photodiodes (Photo detectors)**:-

   Light enters through transparent window in a diode at depletion layer. Photons having energy more than Energy Gap of semiconductor cause electron-hole generation. High intensity of light means high current. This principle can be used for "light intensity meter" (i.e. lux meter) used by umpires in cricket match.



2. **Light Emitting Diode (LED)**:-

   When a diode is forward biased, electron hole combination takes place at *P-N* junction. Photons are ejected from transparent window as e-h combination takes place. If these photons have energy 1.8ev to 3.0ev, it appears as RED. YELLOW, BLUE light. LED has advantage of low voltage, low power, fast action, mono colour, long life etc.

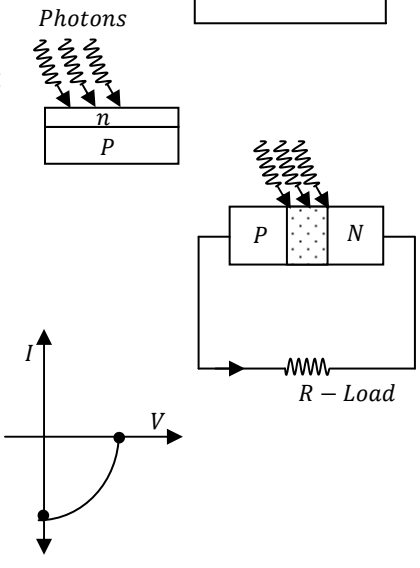


3. **Solar Cell**:-

   Solar Cell converts light (Sun Light) to electricity. It works on same principle as photodiode but no external bias is applied across it.

   a) As light falls, *e-h* pairs are generated.
   b) Electric field of depletion layer forces electrons to *n* side and holes to *p* side.
   c) Electrons and holes are collected at two ends.

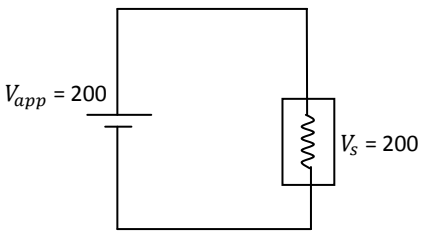
   The above arrangement is used to generate electricity for satellites. *V-I* characteristic of a solar cell is as shown in fig.



b) **Normal Circuit**:

If applied voltage increases from 200 to 220 (say), load is also subjected to 220 volt and may get damaged.

Fig. I



Problem:

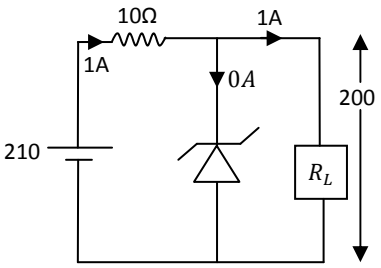
Voltage changes and can damage load.

Zener Diode:

Reverse Bias mode

Under normal voltage conditions say 200 volt, Zener current is 0A and load current is 1A

Fig. II



I_{total} = I_{zener} + I_{load}

= 0 + 1

I_{total} = 1 amp

Voltage drop across 10Ω resistance

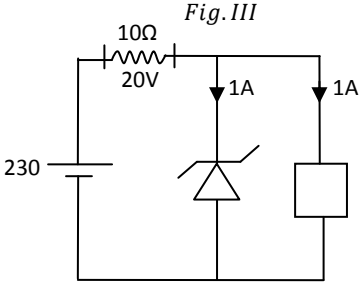
= (10Ω) (1A)

= 10 volt

V_{load} = 210 - 10

= 200 V_{olt}

Fig. III



When voltage increase (say 230 volt) as shown in Fig.III, current through zener increase to 1A (say)

I_{total} = I_{zener} + I_{load}

= 1 + 1

I_{total} = 2 amp

Voltage drop across 10Ω resistance

= (10Ω) (2A)

= 20 V_{olt}

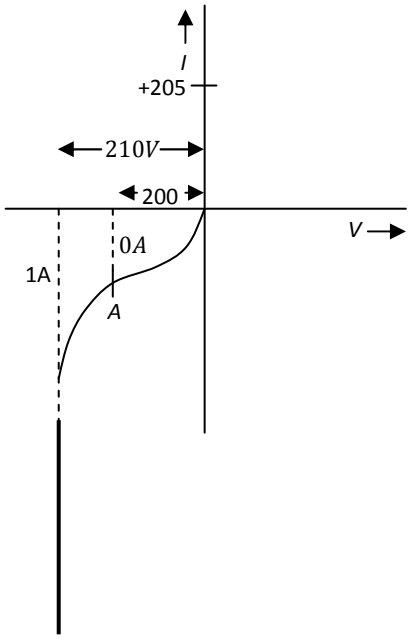
So, V_{load} = 230 - 20

V_{load} = 210 V_{out}

So, Voltage across load increase only by 210-200 = 10 V_{olt}

When supply voltage has increased by 230-210 = 20 V_{olt}

Fig. IV



$210V$

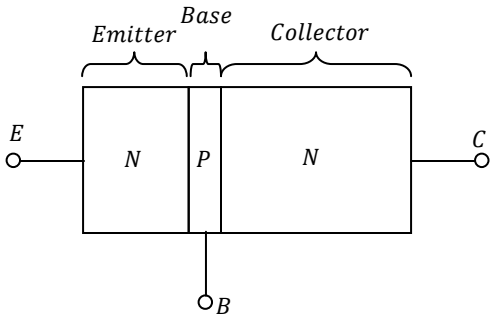
Fig. IV

Q6. a) Transistor, construction, symbol
b) Current relation, value of α and β.

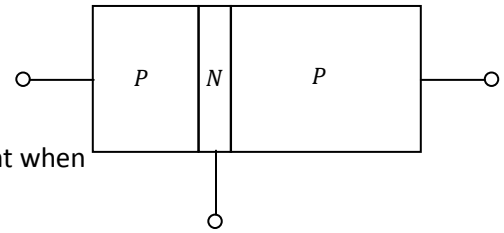
Ans.

a) **Construction**:

1. Transistor is a three terminal, two junction device.
2. It is of two types
   - i) N – P – N or (high use)
   - ii) P – N – P
3. SIZE: Collector > Emitter > Base
4. DOPING: Emitter > Collector > Base

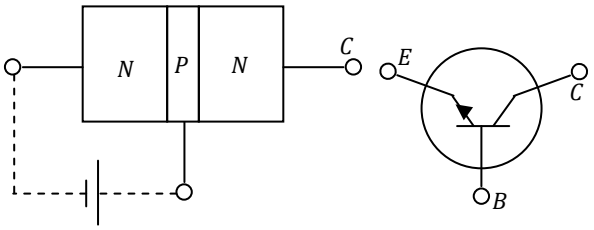


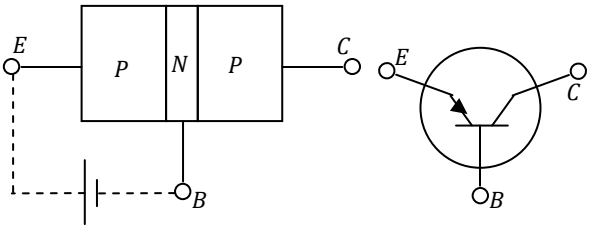
OR



Symbol:

Direction of arrow is flow of conventional current when Base Emitter junction is forward Biased.





b) In working of a transistor, Base – emitter junction is forward Biased Base – collector junction is reverse biased. Forward Biased B-E junction, depletion layer width (d_1). Reverse Biased B – C junction, depletion layer width is large (d_2).

Some of the Electrons moving from emitter to collector are lost due to combination of electrons and holes in base region.

It is because of this reason I_C is less than I_E.

i.e. $I_C < I_E$

As per Kirchoff's current law,

total current entering = total current leaving

$$I_E = I_C + I_B \quad \text{——} (1)$$

100% 98% 2%

α $\alpha = \frac{I_C}{I_E}$ —— (2) $(less\ than\ 1\ and\ \simeq 1)$

$\frac{98}{100} = 0.98$

β $\beta = \frac{I_C}{I_B}$ —— (3) $(more\ than\ 1$

Relation between α and β, divide Eqt. (1) by I_C

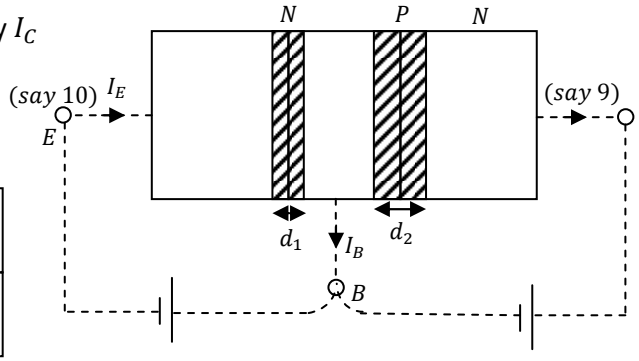
$$\frac{I_E}{I_C} = \frac{I_C}{I_C} + \frac{I_B}{I_C}$$

$$\frac{1}{\alpha} = 1 + \frac{1}{\beta}$$

$$\frac{1}{\alpha} = \frac{\beta + 1}{\beta}$$

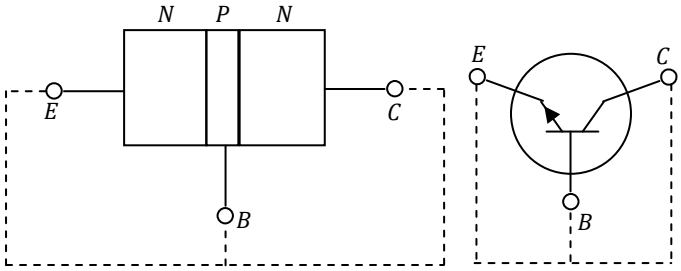
$$\alpha = \frac{\beta}{\beta + 1}$$

$$\beta = \frac{\alpha}{1 - \alpha}$$



Q7. Draw circuit arrangement for CB (Common Base), CE (Common Emitter) and CC (Common Collector) configuration.

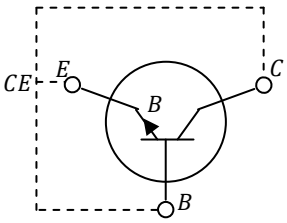
Ans. **<u>CB (Common Base)</u>**:



Base is common to two circuits (input, output)

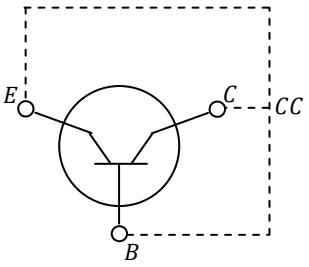
<u>CE (Common Emitter)</u>:

E → Emitter is common to two sides



<u>CC (Common Collector)</u>:

C → Collecter is common to two sides



Q8. Discuss/Plot

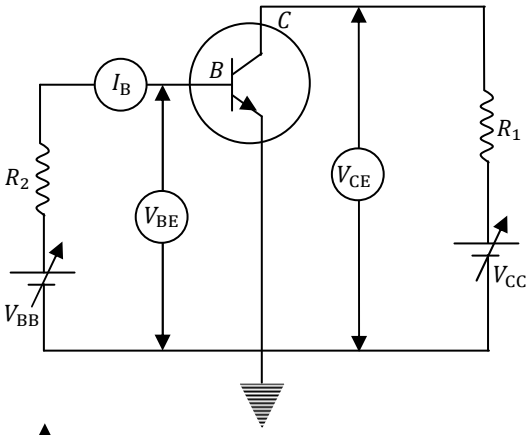
a) Input characteristics of CE transistor

b) **Output characteristics of CE amplifier.**

Ans.

a) **<u>Input Characteristics</u>**:

Input Characteristics is same as that of forward Biased diode. If voltage V_{CE} is increased from 5V to 20V the graph shifts to new position (dotted).

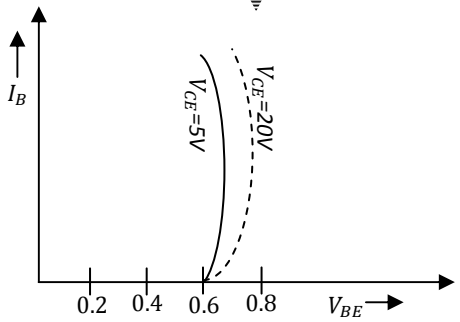


Reason:

As V_{CE} increase, voltage across collector emitter reverse biased junction increases. Depletion layer width increase.

Opposition to flow of I_b also increase. So,

$I_b \rightarrow$ decreases

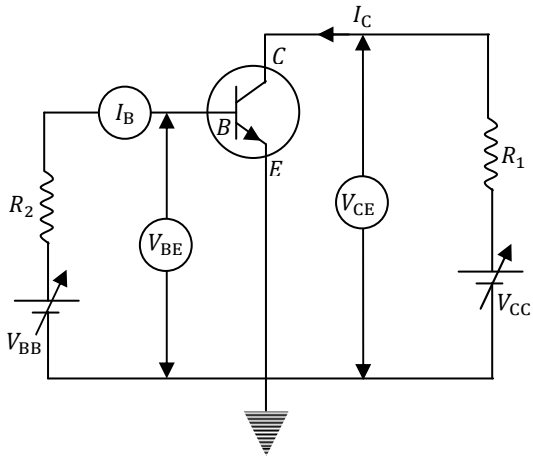


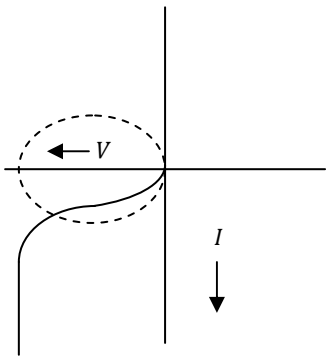
b) **<u>Output characteristics</u>**:

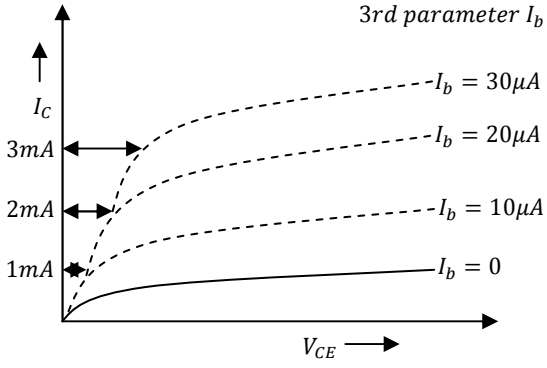
Output characteristics is almost same as that of reverse biased diode.

If I_b is increased, new graph shifts upward.

As I_b increases, conductivity of area increase, which causes increase in I_c $(I_c \, \alpha \, I_b)$.

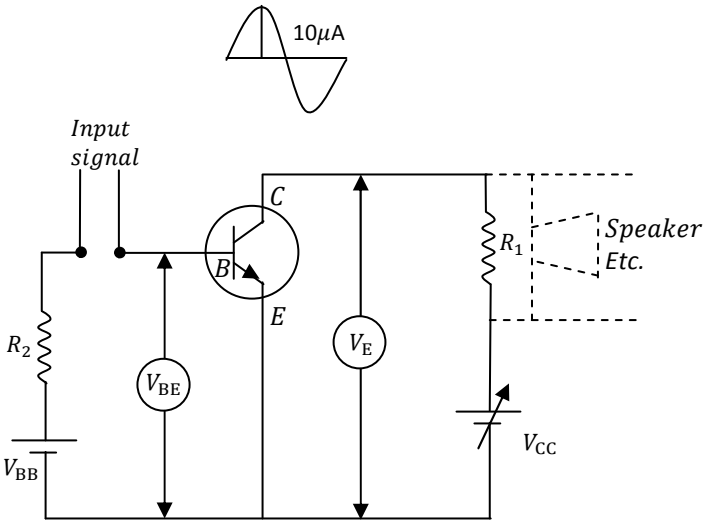






Q9. Explain working of CE amplifier?

Ans. Corresponding to Base current of 20 μA, I_c is $2mA$.
Input signal of 10 μA is given to increase the base current from 20 μA to 30 μA. (As shown in characteristics).



ΔI_b = 10 μA

and

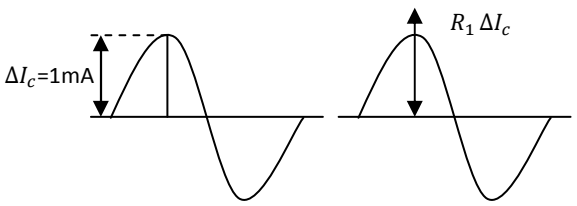
ΔI_c = 1 mA

As shown in characteristics, current gain

$$\frac{\Delta I_c}{\Delta I_b} = \frac{10^{-3}}{10 \text{ x } 10^{-6}}$$

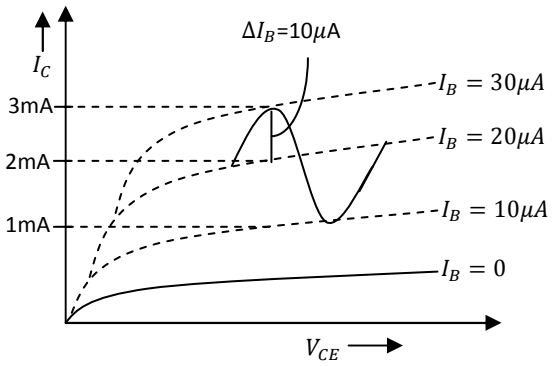
$$= \frac{10^{-4}}{10^{-6}}$$

= 100



<u>Output Current Variation</u>:

Output Current Variation is 100 times input current variation, this principle can be used to amplify current, voltage and power.



Q10. What is

a) Voltage gain in CE amplifier?

b) Current gain in CE amplifier?

c) Power gain in CE amplifier?

Ans.

a) **Voltage gain, A_V** $= \frac{\Delta V_{out}}{\Delta V_{input}}$

$= \frac{R_o(\Delta I_c)}{R_{in}(\Delta I_b)}$

$= \left(\frac{R_o}{R_{in}}\right)\left(\frac{\Delta I_c}{\Delta I_b}\right)$

Voltage gain = (resistance gain) (current gain)

b) **Current gain, β**:

$\beta_{ac} = \frac{\Delta I_c}{\Delta I_b}$

$= \frac{output\ change\ in\ current}{input\ change\ in\ current}$

$\beta = \frac{\Delta I_c}{\Delta I_b}$

c) **Power gain**:

$A_p = \frac{\Delta P_{out}}{\Delta P_{in}}$

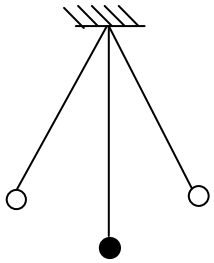
= (voltage gain) (current gain)

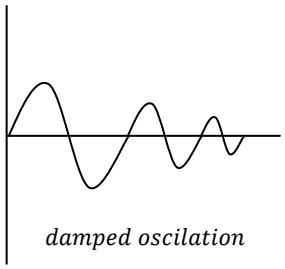
Power gain = $A_V \,.\, \beta$

Q11. Transistor as an oscillator?

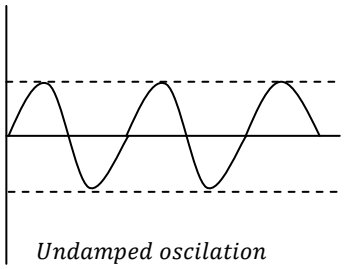
Ans. **Mechanical Oscillator**:-

If a pendulum (or a swing) is taken to one side, it's oscillation die down due to losses. Such oscillation are called damped oscillations. If we give energy at regular intervals to a swing, we can maintain same amplitude for infinite time. These oscillation are termed as undamped oscillations.





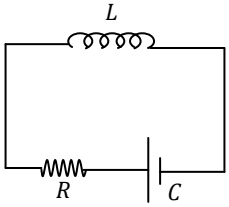
damped oscilation



Undamped oscilation

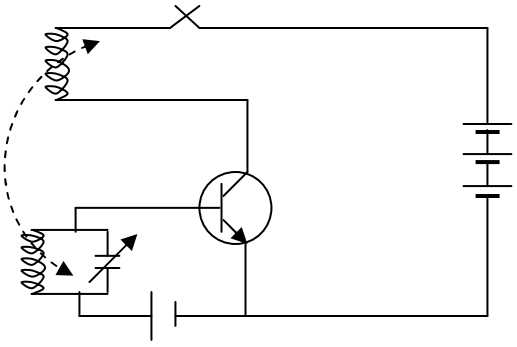
Electric Oscillator:

Similarly, *L*-*C* circuit gives oscillations. These oscillations die down due to loss of energy across resistance of circuit.



A transistor is used to maintain oscillations as shown in fig.

Inductance coil in base circuit is magnetically coupled with inductance coil in collector circuit. As and when energy decreases in *L*-*C* oscillator, it is provided through magnetically coupled coil in collector circuit.



Q12. Transistor as a switch?

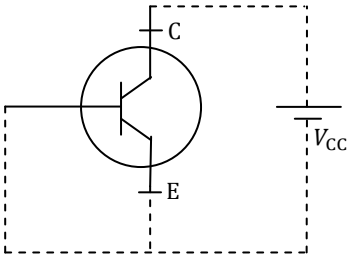
Ans. **Case I**:

SWITCH OFF

I_b = 0

I_c $\simeq$ 0

V_{CE} = V_{CC}



Case II:

SWITCH ON

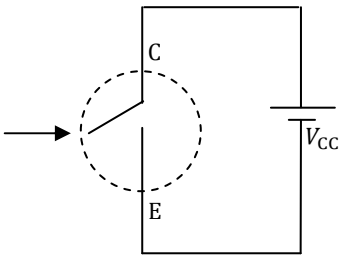
V_{CC} = V_{CE} + I_cR_c

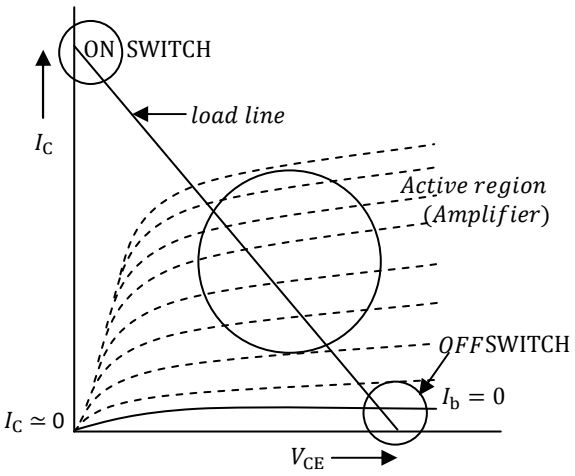
V_{CE} = V_{CC} - I_cR_c

Decrease Increase

As I_c becomes large,
V_{CE} approaches → zero.

Transistor is in "ON mode"





<u>Concept Example</u>:

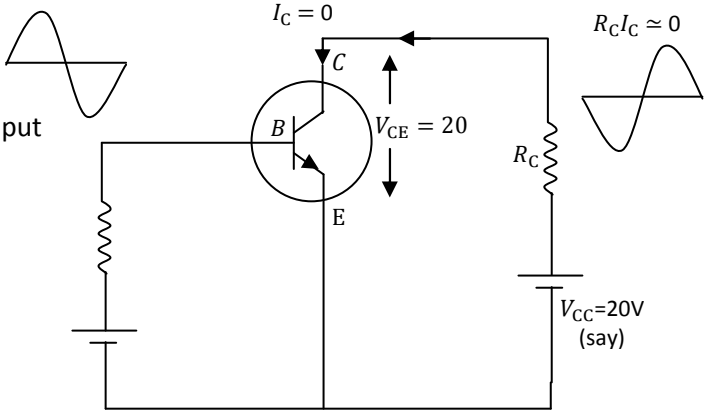
Phase relation in common emitter amplifier

V_{CC} = V_{CE} + I_cR_c

V_{CC} - I_cR_c = V_{CE}

V_{CE} = 20 - I_cR_c

Output = V_{CE} is out of phase the input by 180^0.



Unit – 9C(Logic Gates)

Q1. Use NAND Gate to make

a) NOT GATE

b) AND GATE

c) OR GATE

Ans.

a) **NOT GATE**:

A	Y
0	1
1	0

A	Y
0	1
1	0

b) **AND GATE**:

c) OR GATE

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

Concept Circuit

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

Q2. Use NOR Gate to make

a) NOT GATE

b) AND GATE

c) OR GATE

Ans.

a) NOT GATE

A	Y
0	1
1	0

b) AND GATE

A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

c) OR GATE

Q3. De-Morgan's theorem?

Ans. $\overline{A + B} = \bar{A} \, . \, \bar{B}$

$\overline{AB} = \bar{A} + \bar{B}$